IN THE CLAIMS:

Please amend claim 1 as follows:

Claim 1 (Currently Amended): A method of programming a multi-level flash memory using a sensing circuit that includes a comparator, a reference current supply unit, a sense amplifier driving determining circuit, and a register array, the method comprising:

a data storing step of storing data, in [[a]] each register which is included in each memory cell, corresponding to a level to be programmed;

a first ~~second level~~ program step of, after a first program voltage is applied to word lines, ~~turning off the sensing circuit~~ not performing a program to maintain [[a]] threshold ~~voltage~~ voltages of memory cells ~~at a first level voltage when~~ each of which ~~the data stored in the~~ register having ~~is a first memory cell being~~ a first data, at a first level and performing a program to raise [[the]] threshold ~~voltage~~ voltages of ~~to a second level when the data stored in the register is a~~ remaining memory cells each of which register [[is]] not having ~~other than~~ the first data, to a second level;

a second ~~third level~~ program step of, after a second program voltage is applied to the word lines, ~~turning off the sensing circuit~~ not performing a program to maintain [[the]] threshold ~~voltage~~ voltages of memory cells ~~when the data stored in the~~ each of which register [[is]] having one of ~~the first being~~ the first data or ~~and a second memory cell being~~ a second data, and performing a program to raise [[the]] threshold ~~voltage~~ voltages of ~~to a third level when the data stored in the register is a~~ remaining memory cells each of which [[is]] not having ~~other than~~ one of the first [[and]] or second data, to a third level; and

a third ~~fourth level~~ program step of, after a third program voltage is applied to the word lines, ~~turning off the sensing circuit~~ not performing a program to maintain [[the]] threshold ~~voltage~~ voltages of memory cells ~~when the data stored in the~~ each of which register [[is]] having one of ~~the first memory cell being~~ the first data, ~~the second memory cell being~~ the second data, and ~~a third memory cell being~~ a third data, and performing a program to raise [[the]] threshold ~~voltage~~ voltages of ~~to a fourth level when the data stored in the register is a~~ remaining memory cells ~~is other than~~ not having one of the first data, the second data, and the third data, to a fourth level.

Claim 2 (Previously Presented): The method according to claim 1, wherein the first data is "11," the second data is "10," the third data is "01," and the fourth data is "00."

Claim 3 (Previously Presented): The method according to claim 1, wherein the register includes a number of bits that represent all numbers of levels by which the memory cells can be programmed so that data on the level to be programmed is stored.

Claim 4 (Previously Presented): The method according to claim 1, wherein the sensing circuit is turned OFF and ON by the sense amplifier driving determining circuit depending on the first to fourth data stored in the register.

Claim 5 (Previously Presented): The method according to claim 1, further including an automatic verification program method, wherein an operation of the automatic verification program method is stopped at a time when the threshold voltage of the memory cells becomes higher than a reference cell of the reference current supply unit by comparing a reference current generated in the reference current supply unit with a drain current of the memory cells using the comparator.

Claim 6 (Previously Presented): The method according to claim 1, wherein the first to third program voltages applied to the word lines are a medium voltage of each of the threshold voltages, and are sequentially applied from a low voltage.

Claim 7 (Withdrawn): A method of reading a multi-level flash memory using a sensing circuit that includes a comparator, a voltage regulating block, a reference current supply unit, a sense amplifier driving determining circuit, a register array, and a counter, the method comprising:

a first initialization step of setting to store a fourth data in a plurality of registers, apply a first read voltage to word lines, and output a first data to the counter;

a first read step of sequentially comparing a first reference current of the reference current supply unit with a drain current of a plurality of memory cells in the comparator, and then storing a first data at a corresponding register to define a first memory cell when a threshold voltage is lower than a reference cell, and maintaining the fourth data stored in the register to

complete a read operation of the first memory cell when the threshold voltage is lower than the reference cell;

a second initialization step of setting to apply a second read voltage to the word lines, and to allow the counter to output a second data;

a second read step of sequentially comparing a second reference current of the reference current supply unit with a drain current of the plurality of memory cells in the comparator only when the first memory cell is not read, and then storing the second data at a corresponding register to define a second memory cell when the threshold voltage is lower than the reference cell, and maintaining the fourth data stored in the register to complete the read operation of the second memory cell when the threshold voltage is lower than the reference cell;

a third initialization step of setting to apply a third read voltage to the word lines, and to allow the counter to output a third data; and

a third read step of sequentially comparing a third reference current of the reference current supply unit with a drain current of the plurality of memory cells in the comparator only when one of the first and second memory cells is not read, and then storing the third data at a corresponding register to define a third memory cell when the threshold voltage is lower than the reference cell, and maintaining the fourth data stored in the register to complete the read operation of the third and fourth memory cells when the threshold voltage is lower than the reference cell.

Claim 8 (Withdrawn): The method according to claim 7, wherein the register includes a number of bits that represent all numbers of levels by which the memory cells can be programmed to allow more than 2 bits to be stored when data in the multi-bit flash memory cell is more than 2 bits.

Claim 9 (Withdrawn): The method according to claim 7, wherein the sense amplifier driving determining circuit determines whether the sensing circuit has to be driven depending on the data stored in the register.

Claim 10 (Withdrawn): The method according to claim 7, wherein the first to third read voltages applied to the word lines are sequentially applied from a low voltage, and each correspond to a medium voltage of the threshold voltage levels.

Claim 11 (Withdrawn): The method according to claim 7, wherein the first data is "11," the second data is "10," the third data is "01," and the fourth data is "00."

Claim 12 (Withdrawn): The method according to claim 7, wherein the third read step detects only data of upper bits among data stored in the register, and then determines them to be one of the first and second memory cell when the data of upper bits is "1" to be remaining cells when the data of upper bits is "0."

Claim 13 (Withdrawn): The method according to claim 7, wherein the sensing circuit is turned OFF and ON by the sense amplifier driving determining circuit depending on the first to fourth data stored in the register.